IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1. (Currently Amended) A method of forming an integrated circuit transistor having a reduced gate height, said method comprising:

forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor;

patterning said laminated structure into at least one gate stack extending from said substrate;

forming spacers to have a target spacer width adjacent said gate stack;

doping regions of said substrate not protected by said spacers with a dopant to form source and drain regions adjacent said gate stack, wherein said target spacer width controls an amount of diffusion of said dopant into a channel region of said substrate below said gate conductor; and

removing said spacers and said sacrificial layer.

2. (Currently Amended) The method in claim 1, wherein ~~the height of said gate conductor is smaller than a gate height associated with the spacing of the source and drain regions created by said spacers~~ said forming of said spacers adjacent said gate stack comprises forming said spacers adjacent said gate conductor and said at least one sacrificial oxide layer above said gate conductor.

3. (Currently Amended) The method in claim 1, wherein the size of said spacers is controlled by the height of said gate stack and wherein by forming said gate stack from ~~combined height of~~ said gate conductor and said sacrificial layer, as opposed to from said gate conductor alone, a height of said gate stack can be increased so that said size, including a width, of said spacers can be modulated to form larger spacers, ~~such that said spacers provide larger spacing for said combined height when compared to the height of said gate conductor alone~~.

4. (Currently Amended) The method in claim 3, wherein forming of said larger spacers ~~said larger spacing~~ positions said source and drain regions further from said gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor.

5. (Currently Amended) The method in claim 1, wherein said sacrificial layer above said gate conductor is formed in a process comprising:

forming a sacrificial oxide layer above said gate conductor, and

forming additional sacrificial layers above said oxide layer.

6. (Original) The method in claim 5, wherein said sacrificial oxide layer protects said gate conductor.

7. (Currently Amended) The method in claim 1, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises doping said ~~source/drain electrodes~~ source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and said gate dielectric layer to said silicon layer.

8. (Currently Amended) The method in claim 1, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises a first doping process of doping ~~source/drain electrodes~~ said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process,

wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and said gate dielectric layer to said silicon layer.

9. (Currently Amended) A method of forming an integrated circuit transistor having a reduced gate height, said method comprising:

forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor;

patterning said laminated structure into at least one gate stack extending from said substrate;

forming spacers to have a target spacer width adjacent said gate stack;

epitaxially growing raised source and drain regions on said substrate adjacent said ~~gate stack~~ spacers;

after said epitaxially growing of said raised source and drain regions, implanting impurities into said raised source and drain regions and into said substrate below said raised source and drain regions,

wherein implanting said impurities after said epitaxially growing of said raised source and drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process and wherein said said target spacer width controls an amount of diffusion of said impurities into said gate conductor; and

removing said spacers and said sacrificial layer.

10. (Currently Amended) The method in claim 9, wherein the size of said spacers is

controlled by the height of said gate stack and wherein by forming said gate stack from ~~combined height of~~ said gate conductor and said sacrificial layer, as opposed to from said gate conductor alone, a height of said gate stack can be increased so that said size, including a width, of said spacers can be modulated to form larger spacers, ~~such that said spacers provide larger spacing for said combined height when compared to the height of said gate conductor alone~~.

11. (Currently Amended) The method in claim 10, wherein ~~said~~ forming of said larger ~~spacing~~ spacers positions said raised source and drain regions further from said gate conductor when compared to raised source and drain regions formed with spacers formed only to said height of said gate conductor.

12. (Original) The method in claim 9, wherein said sacrificial layer above said gate conductor is formed in a process comprising:

forming a sacrificial oxide layer above said gate conductor, and

forming additional sacrificial layers above said oxide layer,

wherein said sacrificial oxide layer protects said gate conductor.

13. (Currently Amended) The method in claim 9, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises doping said ~~source/drain electrodes~~ source

and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and said gate dielectric layer to said silicon layer.

14. (Currently Amended) The method in claim 9, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises a first doping process of doping ~~source/drain electrodes~~ said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process,

wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and said gate dielectric layer to said silicon layer.

15. (Currently Amended) The method in claim 9, wherein by implanting said

impurities after said epitaxially growing process, said impurities avoid being ~~subjected to the~~ being diffused as a result of said thermal budget of said epitaxially growing process.

16. (Currently Amended) A method of forming an integrated circuit transistor having a reduced gate height, said method comprising:

forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor;

patterning said laminated structure into at least one gate stack extending from said substrate;

forming spacers to have a target spacer width adjacent said gate stack;

epitaxially growing raised source and drain regions on said substrate adjacent said ~~gate stack~~ spacers, wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities;

after said epitaxially growing of said raised source and drain regions, implanting impurities into said raised source and drain regions and into said substrate below said raised source and drain regions,

wherein implanting said impurities after said epitaxially growing of said raised source and drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process and wherein said target spacer width controls an amount of diffusion of said impurities into said gate conductor; and

removing said spacers and said sacrificial layer.

17. (Currently Amended) The method in claim 16, wherein ~~the height of said gate conductor is smaller than a gate height associated with the spacing of the source and drain regions created by said spacers~~ said forming of said spacers adjacent said gate stack comprises forming said spacers adjacent said gate conductor and said at least one sacrificial oxide layer above said gate conductor.

18. (Currently Amended) The method in claim 16, wherein the size of said spacers is controlled by the height of said gate stack and wherein by forming said gate stack from ~~said combined height of~~ said gate conductor and said sacrificial layer, as opposed to from said gate conductor alone, a height of said gate stack can be increased so that said size, including a width, of said spacers can be modulated to form larger spacers, ~~such that said spacers provide larger spacing for said combined height when compared to the height of said gate conductor alone~~.

19. (Currently Amended) The method in claim 18, wherein ~~said~~ forming of said larger ~~spacing~~ spacers positions said source and drain regions further from said gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor.

20. (Original) The method in claim 16, wherein said sacrificial layer above said gate conductor is formed in a process comprising:

forming a sacrificial oxide layer above said gate conductor, and

forming additional sacrificial layers above said oxide layer.

21. (Original) The method in claim 20, wherein said sacrificial oxide layer protects said gate conductor.

22. (Currently Amended) The method in claim 16, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises doping said ~~source/drain electrodes~~ source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and said gate dielectric layer to said silicon layer.

23. (Currently Amended) The method in claim 16, wherein said laminated structure includes a gate dielectric layer below said gate conductor layer and a silicon layer below said gate dielectric layer,

wherein said method further comprises a first doping process of doping ~~source/drain electrodes~~ said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process,

wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process,

wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and

whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and said gate dielectric layer to said silicon layer.

24. (Currently Amended) A method of producing an integrated circuit transistor comprising:

forming a laminated stack deposition,

wherein said laminated stack deposition is formed in a process comprising:

forming a silicon layer over a substrate layer;

forming a gate oxide on said silicon layer;

forming a gate conductor on said gate oxide; and

forming of least one sacrificial material above said gate conductor,

patterning said gate oxide, gate conductor, and said sacrificial material into at least one gate stack;

forming temporary spacers to have a target spacer width adjacent said gate stack;

epitaxially growing raised source and drain regions above said substrate layer adjacent said temporary spacers, such that said temporary spacers separate said raised source and drain regions from said gate stack;

simultaneously implanting impurities into said raised source and drain regions and into said substrate below said raised source and drain regions,

wherein implanting said impurities after said epitaxially growing of said raised source and drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process and wherein said target spacer width controls an amount of diffusion of said impurities into said gate conductor;

growing an additional dielectric layer on said raised source and drain regions;

removing said temporary spacers without removing all of said sacrificial material;

performing a halo implant in said raised source and drain regions and in exposed regions of said silicon layer;

forming a permanent spacer adjacent said gate stack, wherein said permanent spacer is thinner than said temporary spacer;

~~implanting impurities into~~ performing a source and drain extensions implant in said raised source and drain regions and exposed regions of said silicon;

forming a final spacer filling said exposed regions of said silicon between said permanent spacer and said raised source and drain regions;

implanting additional impurities into said raised source and drain regions and exposed regions of said silicon;

annealing to activate all impurities;

etching back said additional dielectric layer on said raised source and drain regions; and

saliciding both said gate conductor and said raised source and drain regions.

25. (Original) The method in claim 24, wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities.

26. (Original) The method in claim 24, wherein said removing of said sacrificial layer reduces the height of said gate conductor relative to the gate height associated with the spacing of the source and drain regions created by said spacers.

27. (Original) The method in claim 24, wherein said forming of said sacrificial material above said gate conductor further comprises forming a sacrificial oxide layer above said gate conductor, forming a sacrificial nitride layer above said oxide layer and forming a sacrificial hard insulator material above said nitride layer.

28. (Currently Amended) The method in claim [[31]] 24, wherein said sacrificial oxide layer protects said gate conductor.